REMARKS

Reconsideration of the above identified application in view of the preceding amendments and following remarks is respectfully requested. Claims 1, 2, 4, 5 and 13 are pending in the present application. Claims 1, 2, and 5 have been amended herein and Claims 10-12 have been cancelled. It is respectfully submitted that no new matter has been introduced by these amendments, as support therefor is found throughout the specification and drawings.

I. PRIOR ART REJECTIONS

A. Claims 1, 2, 4, 10, 11, and 13

Claims 1, 2, 4, 10, 11, and 13 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,773,996 (Suzawa). This rejection is traversed.

Suzawa discloses a method for reducing the number of photoresist masks required in order to reduce the cost of semiconductor manufacturing. Critical to accomplishing this goal is forming self-aligning structures (see col. 3, lines 16-24). The self-aligning structures are tapered gate electrodes. The tapered gate electrode is used as a mask such that an impurity is doped with self-alignment (see col. 4, line 31 to col. 5, line 6). Suzawa defines a taper angle as the sloping face of a conducting layer sidewall. By controlling bias power, Suzawa is able to form a taper angle between 5 to 80 degrees. Suzawa achieves taper angles of "70° to 80° and thus the shape of the edge of the W film is *almost vertical*" (see col. 11, lines 6-11,

emphasis added). By almost vertical, it is apparent that Suzawa means up to 80° but no steeper. Suzawa was not able to achieve a taper angle above 80° nor does it suggest such an accomplishment. In short, Suzawa failed to create or even mention of suggest a taper angle above 80°.

There is nothing in Suzawa that discloses or suggests the device defined by the Claims of the subject application.

In particular with respect to Claim 1, there is nothing in Suzawa which discloses or suggests, a process of manufacturing a semiconductor device including forming an insulating layer above a semiconductor layer, forming a conductive layer including a tantalum layer and a tantalum nitride layer, the conductive layer having a sidewall and etching the conductive layer by using a gas including $SiCl_4$ and NF_3, wherein; a reactive material accumulates in the sidewall of the conductive layer to function as protection and the ratio of the flow rate of the NF_3 to the flow rate of the sum of the $SiCl_4$ and the NF_3 is approximately 1 to approximately 30 % such that an angle between the sidewall of the etched conductive layer and the insulating layer is 85 to 90 degrees. Consequently, Claim 1 teaches a range of taper angle above anything Suzawa contemplated or suggested. In other words, despite Suzawa's comprehensive testing results, it failed to produce such a taper angle. Unlike *In re Woodruff* cited by the Examiner, there is no overlap between the claimed range and that disclosed by Suzawa. Moreover, the particular parameters recited in Claim 1 are critical to achieve the difficult limitation of the 85 to 90

degree sidewall. Thus, Claim 1 is not obvious because of the unique range and critical parameters required to achieve it.

Further still, Claim 1 recites a reactive material accumulates in the sidewall of the conductive layer to function as protection and Suzawa forms no such protection. Therefore, for at least these reasons, Claim 1 and Claim 4 depending therefrom are not rendered obvious by Suzawa, and withdrawal of the rejection under 35 U.S.C. §103 (a) is respectfully requested.

Turning to Claim 2, there is nothing in Suzawa which discloses or suggests, a process of manufacturing a semiconductor device including, *inter alia*, etching the conductive layer by using a gas including NF_3 and C_2F_6 such that approximately 70-80% of the tantalum layer and the tantalum nitride layer are etched and subsequently etching the conductive layer again by using a gas including $SiCl_4$ and NF_3, wherein; the ratio of the flow rate of the NF_3 to the flow rate of the sum of the $SiCl_4$ and the NF_3 is approximately 1 to approximately 30 % such that the conductive layer is etched to be approximately 89 degrees. Consequently, Claim 2 not only teaches a taper angle above anything Suzawa contemplated or suggested but also discloses a gas having the component of C_2F_6, which is not used or suggested in Suzawa either. Further still, Claim 2 recites a first partial etching step that is not taught or suggested by Suzawa. Therefore, Claim 2 and Claim 13 depending therefrom are not rendered obvious by Suzawa, and withdrawal of the rejection under 35 U.S.C. §103 (a) is respectfully requested.

Claims 10 and 11 have been cancelled. Thus, the rejection thereto has been obviated.

B. Claims 5 and 12

Claims 5 and 12 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Suzawa in view of JP 2001-298193 (JP '193). This rejection is traversed.

There is nothing in either Suzawa or JP '193 that discloses or suggests the device defined by the Claim 5 of the subject application. In particular, there is nothing in Suzawa or JP '193, which discloses or suggests, either alone or in combination, in whole or in part, a process of manufacturing a semiconductor device including forming an insulating layer above a semiconductor layer, forming a first tantalum nitride layer, body centered cubic lattice phase tantalum layer and a second tantalum nitride layer in this order, forming a gate electrode by etching the first tantalum nitride layer, the body centered cubic lattice phase tantalum layer and the second tantalum nitride layer with using a gas including $SiCl_4$ and NF_3 and forming first and second impurity layers constituting a source region and a drain region through introducing a impurity into the semiconductor layer, wherein; the ratio of the flow rate of the NF_3 to the flow rate of the sum of the $SiCl_4$ and the NF_3 is approximately 1 to approximately 30 % such that the conductive layer is etched to be 90 degrees. Consequently, Claim 5 teaches a 90 degree taper angle well above anything contemplated or suggested by the combination of references cited by the

Examiner. Therefore, Claim 5 is not rendered obvious by the cited combination, and withdrawal of the rejection under 35 U.S.C. §103 (a) is respectfully requested.

Claim 12 has been cancelled. Thus, the rejection thereto has been obviated.

Based on the foregoing, Applicant submits that the present application is in condition for allowance. Applicant kindly requests the Examiner to contact the undersigned at the phone number listed below to discuss this application, if the Examiner feels that such discussion may expedite prosecution of the present application.

Applicant believes that no additional fees are due for the subject application. However, if for any reason a fee is required, a fee paid is inadequate or credit is owed for any excess fee paid, you are hereby authorized and requested to charge Deposit Account No. 04-1105.

Respectfully submitted,

Date: June 27, 2006
Customer No.: 21874

George N. Chaclas (Reg. No. 46,608)
for John J. Penny, Jr. (Reg. No. 36,984)
EDWARDS ANGELL PALMER & DODGE LLP
P.O. Box 55874
Boston, MA 02205
Tel.: (617) 517-5549
Fax: (617) 439-4170